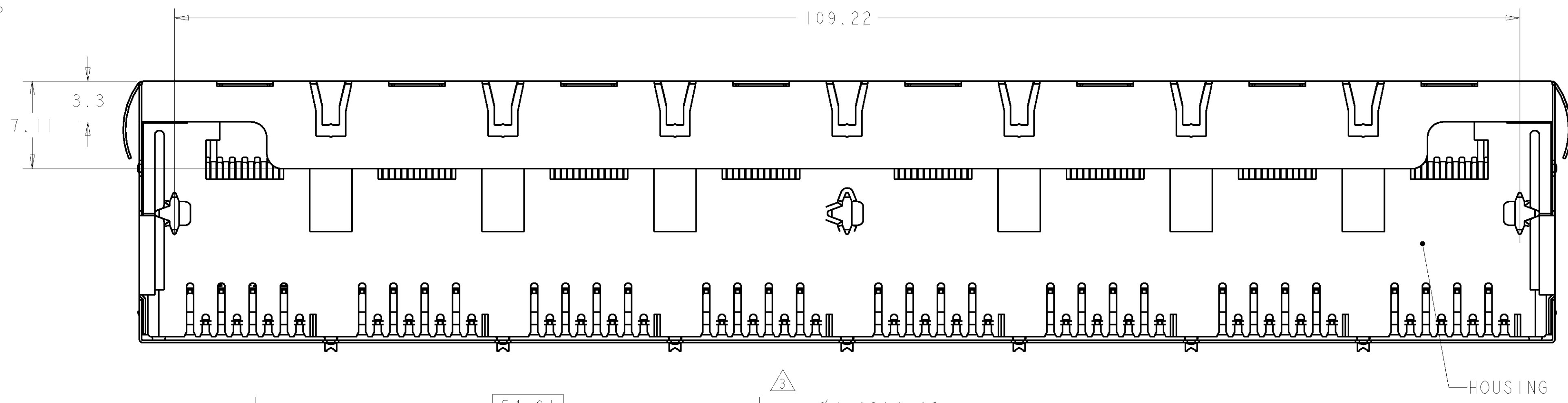
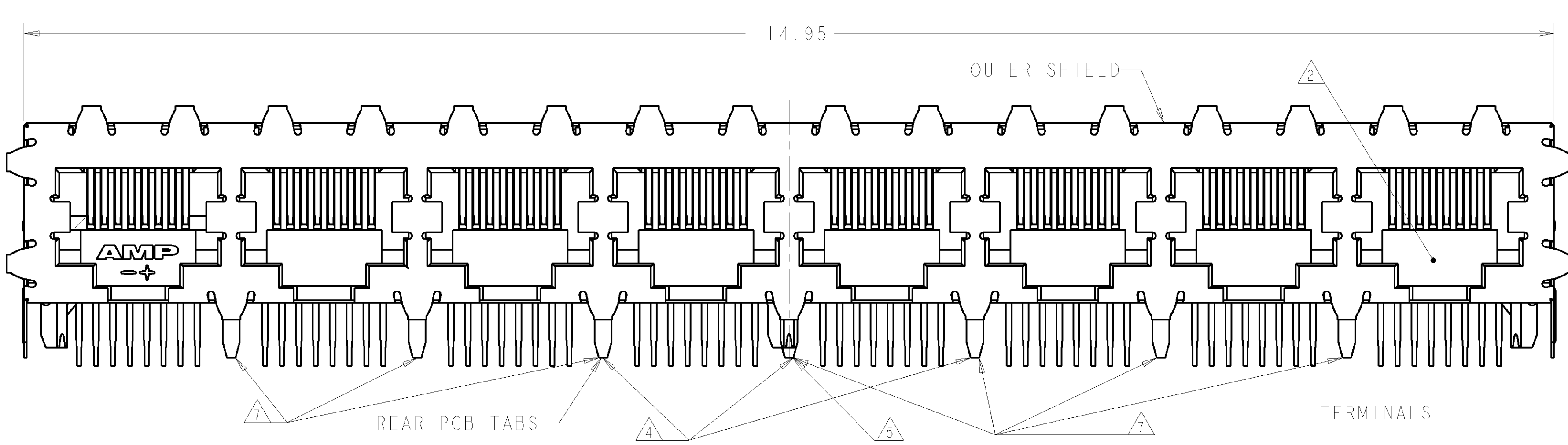
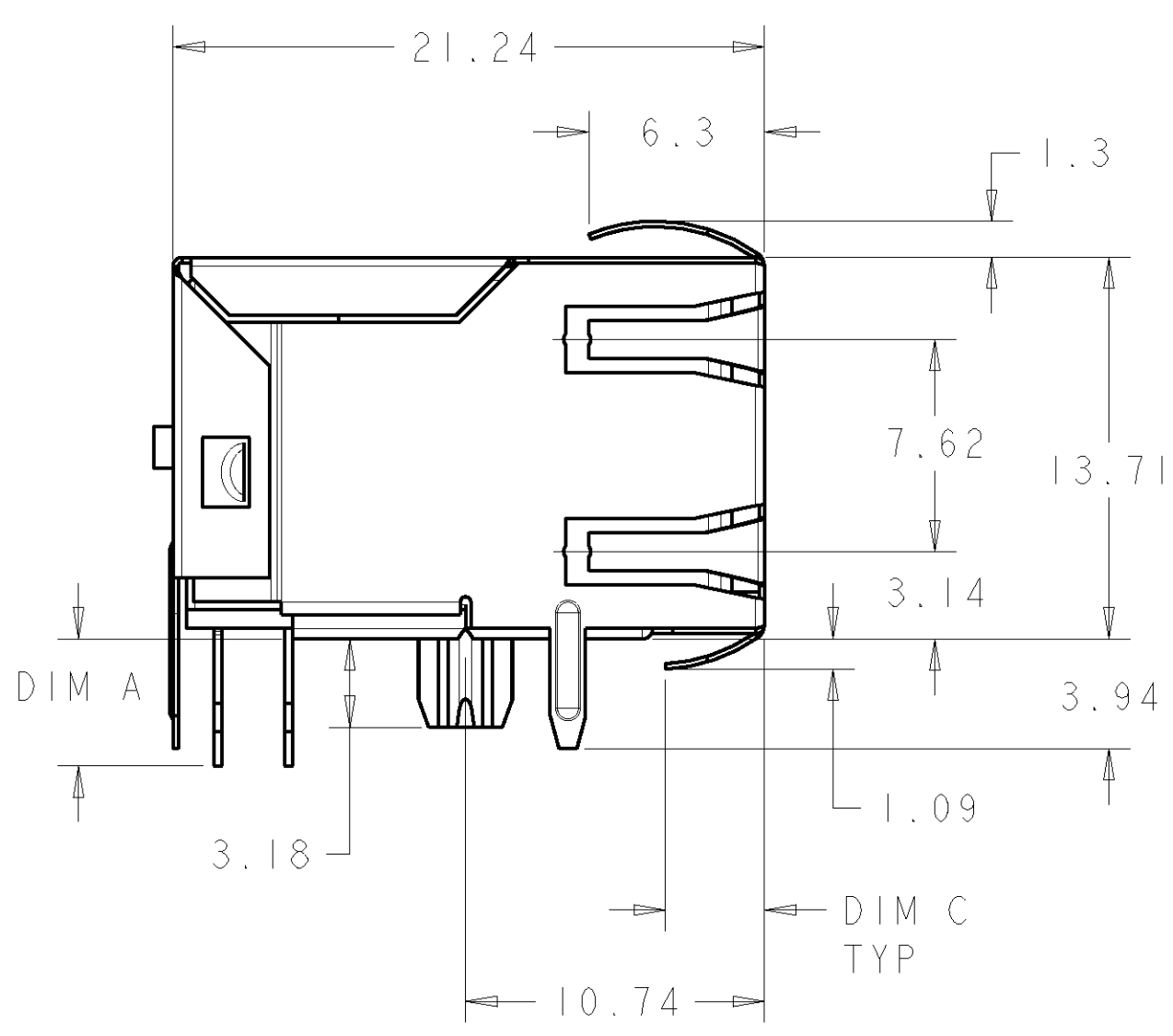
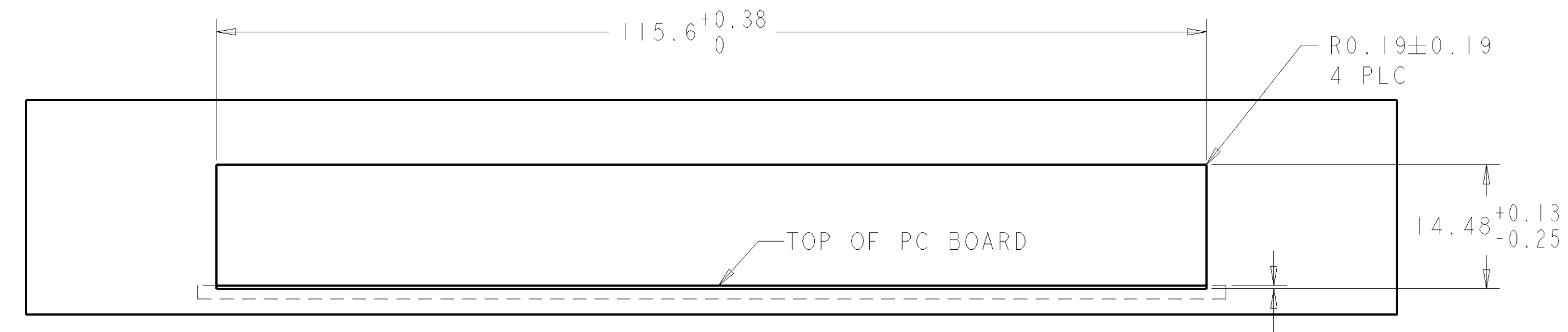
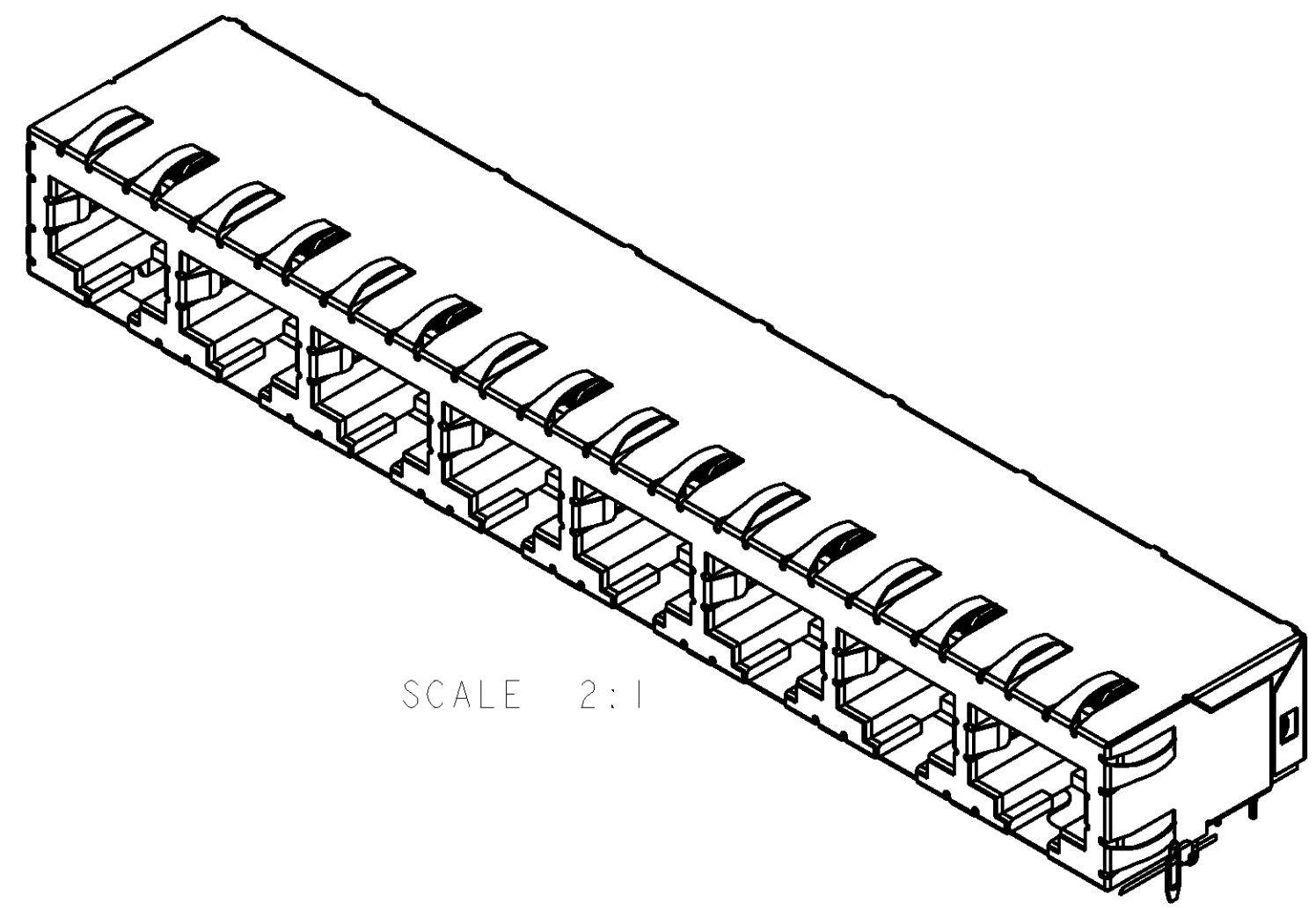
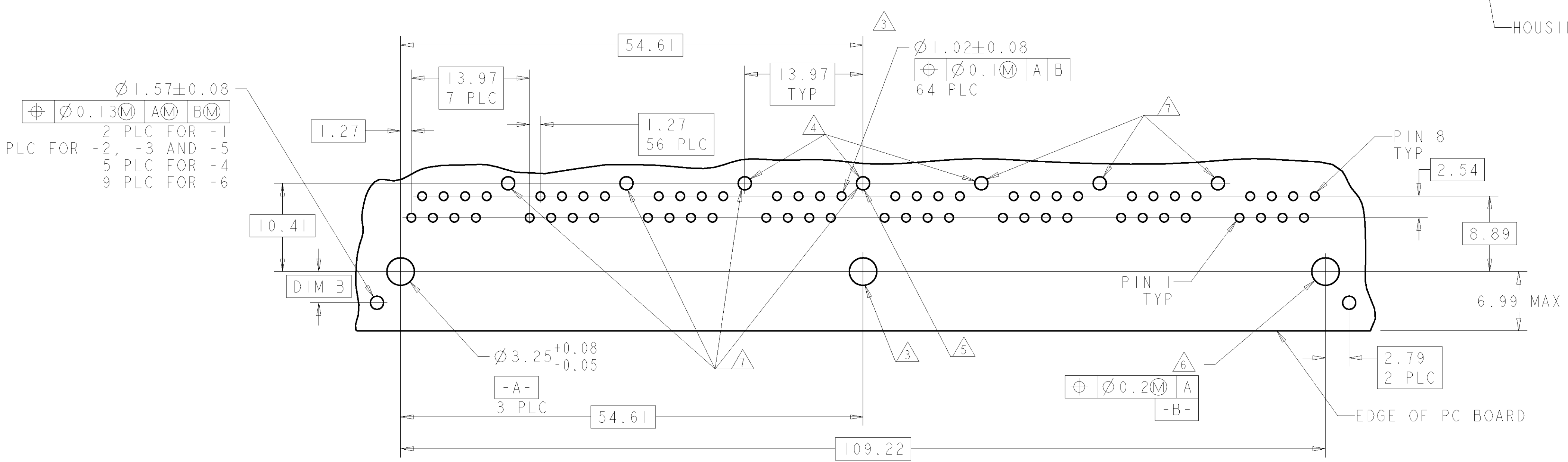


LOC	DIST	REV	DATE	BY	APPD
AA	22				
B3		REVISED PER ECO-11-005033	20APR11	RK	HMR



- △ HOUSING: PCT POLYESTER, BLACK, UL 94V-0. IR REFLOW PROCESS COMPATIBLE.
- TERMINALS: 0.305 THICK PHOS BRONZE PLATED WITH 1.27µm MINIMUM THICK HARD GOLD IN LOCALIZED AREA AND 2.03µm MINIMUM THICK MATTE TIN IN SOLDER AREA OVER 1.27µm MINIMUM THICK NICKEL UNDERPLATE.
- SHIELD: 0.196 THICK COPPER ALLOY PLATED WITH 1.27µm MINIMUM NICKEL AND 2.03µm MINIMUM HOT TIN DIP ON PCB GROUND TABS.
- △ 2 JACK CAVITY CONFORMS TO FCC RULES AND REGULATIONS, PART 68 SUBPART F
- △ 3 CENTER BOARD LOCATOR AND PCB HOLE REQUIRED FOR ALL, EXCEPT -1
- △ 4 PCB HOLES/TABS USED FOR -4
- △ 5 PCB HOLES/TABS USED FOR -2, -3, AND -5
- △ 6 USE #30 DRILL BIT OR 3.25mm DRILL BIT WHEN PRODUCING THESE PCB HOLES
- △ 7 PCB HOLES/TABS USED FOR -6
- 8. RECOMMENDED APPLICATIONS: FAST ETHERNET, 10 BASE-T ETHERNET, AND 10/100 BASE-T ETHERNET (CAT 5 TWO PAIR 1/2, 3/6)
- △ 9 OBSOLETE PARTS: OBSOLETE CIS STREAMLINING PER D.RENAUD/D.SINISI



3.56	3.68	7	3	3.56	6339169-6
3.15	4.57	1	3	3.56	6339169-5
3.56	3.68	3	3	3.56	△ 9 6339169-4
3.56	4.57	1	3	3.56	6339169-3
3.56	3.68	1	3	3.56	6339169-2
3.56	4.57	0	2	3.56	△ 9 6339169-1
DIM C	DIM B	NUMBER OF REAR PCB TABS	NUMBER OF BOARD LOCATORS	DIM A	PART NO.

DIMENSIONS: mm TOLERANCES UNLESS OTHERWISE SPECIFIED: 9 PLC ±.25 8 PLC ±.25 5 PLC ±.25 4 PLC ±.25 ANGLES .45		DWG: L. VARELA - 23 JUN 2005 CHK: J. WESTMAN - 23 JUN 2005 APPD: S. FLICKINGER - 23 JUN 2005 PRODUCT SPEC: 108-1163-9 APPLICATION SPEC: 114-2048 WEIGHT: - CUSTOMER DRAWING		NAME: ASSEMBLY, MULTI-PORT, 1X8, 8 POSITION, SHIELDED, WAVE PANEL GROUND SIZE: 4-1 SHEET: 1 OF 1 REV: B3	
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